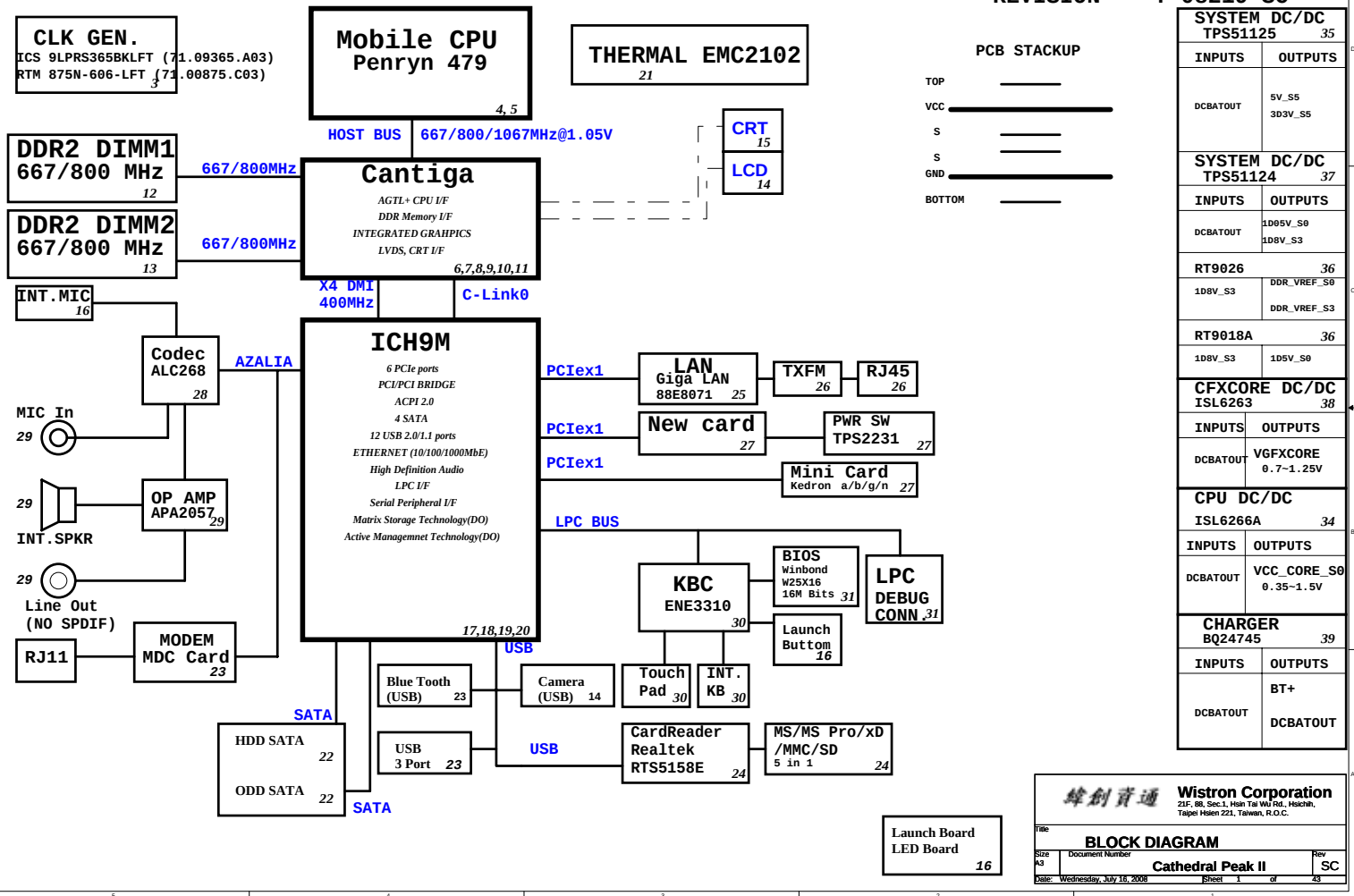


Project code: 91.4K801.001
PCB P/N : 48.4K801.0SC
REVISION : 08219-SC



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Signal	Usage/when Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PwROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PwROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PwROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIe config2 bit2, Rising Edge of PwROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PwROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PwROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FW BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PwROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPwROK	Sample low: The Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage Rising Edge of PwROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PwROK.	Signal has weak internal pull-up. Sets bit 27 of NPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PwROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PwROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PwROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

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SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST#	PULL-UP 20K
DPRSLLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN docks functionality and determined by LAN controller
GNT[3:0]/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CL6PIO6	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

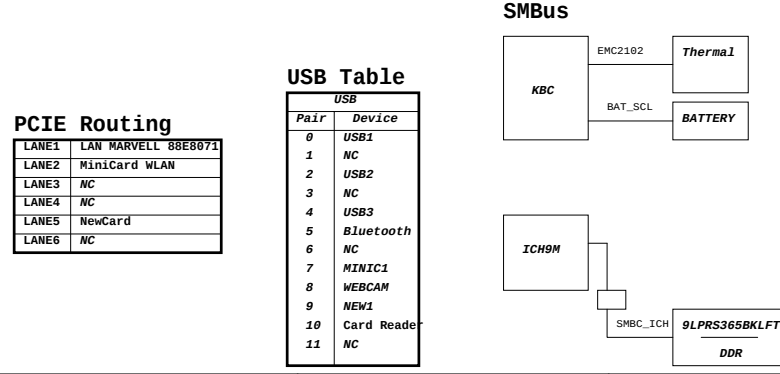
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Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB660 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0= The ITPM Host Interface is enabled(Note2) 1=The ITPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes, 15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 01 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0, 2->1, 1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIe	0 = Only Digital Display Port 1 = or PCIe is operational (Default) 1 = Digital Display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled



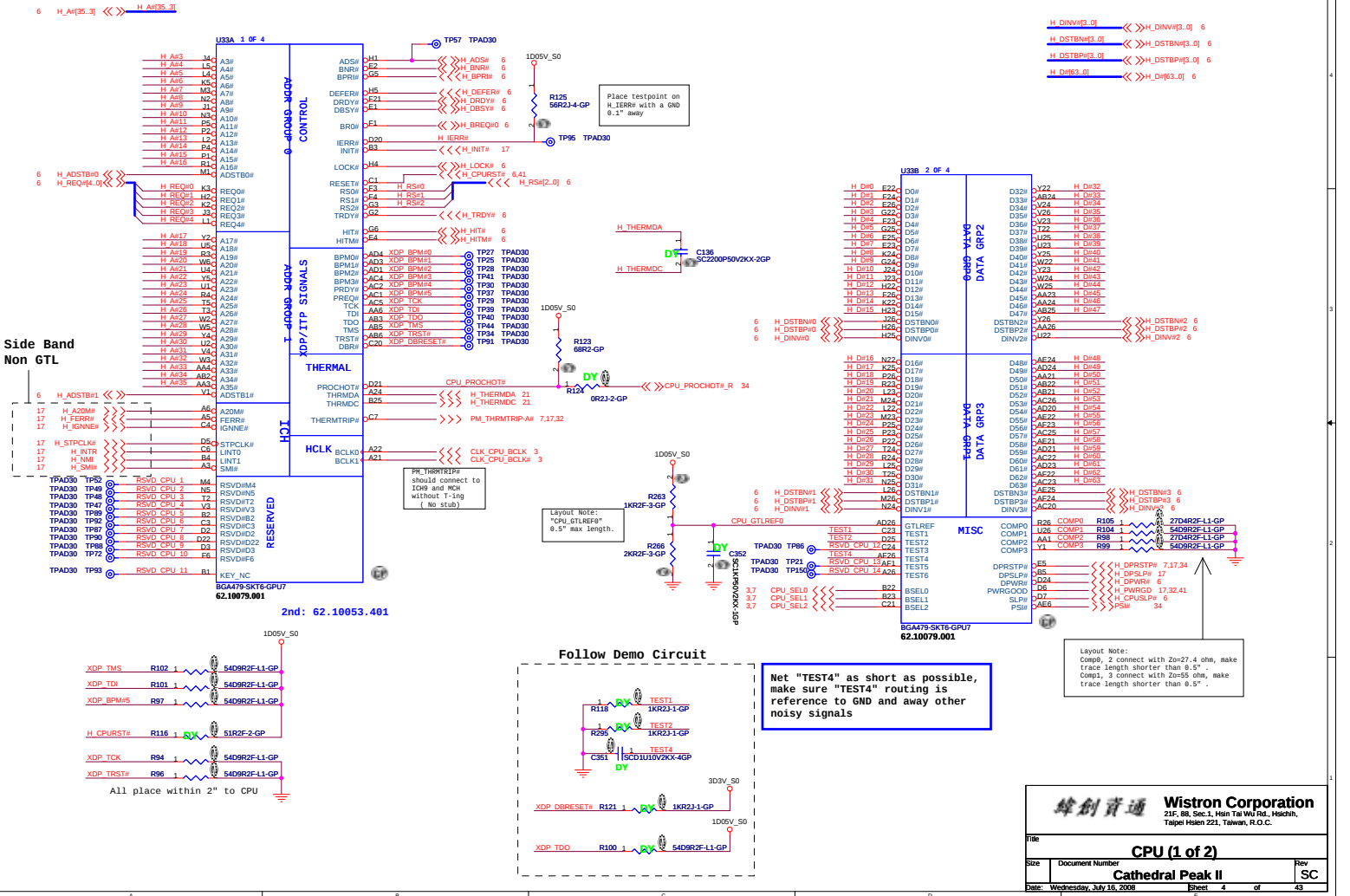
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21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.		
Title		
Reference		
Size A3	Document Number	Rev SC
Cathedral Peak II		
Date: Wednesday, July 16, 2008	Sheet 2 of	43

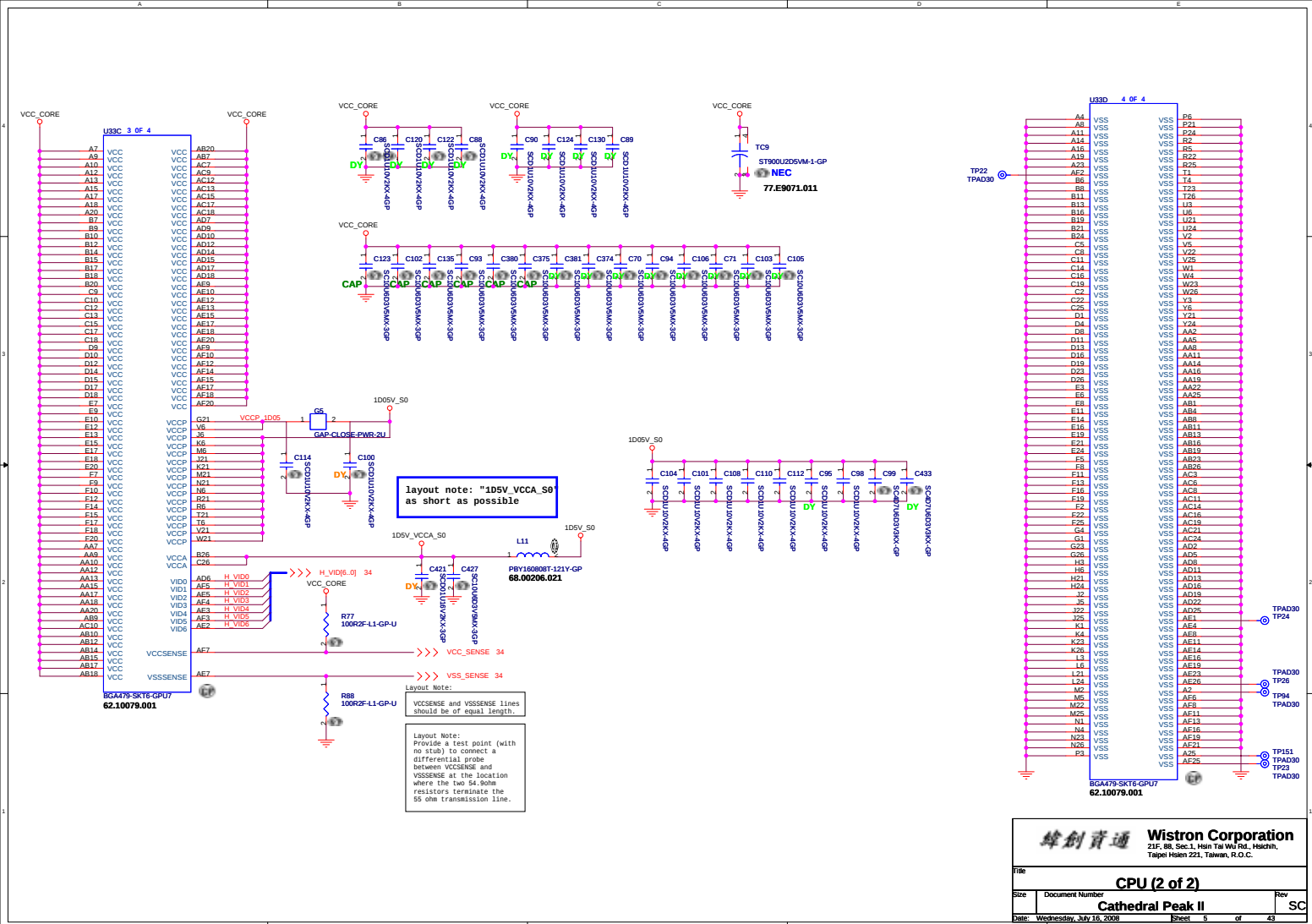


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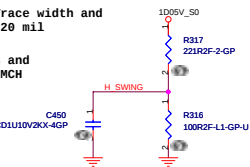
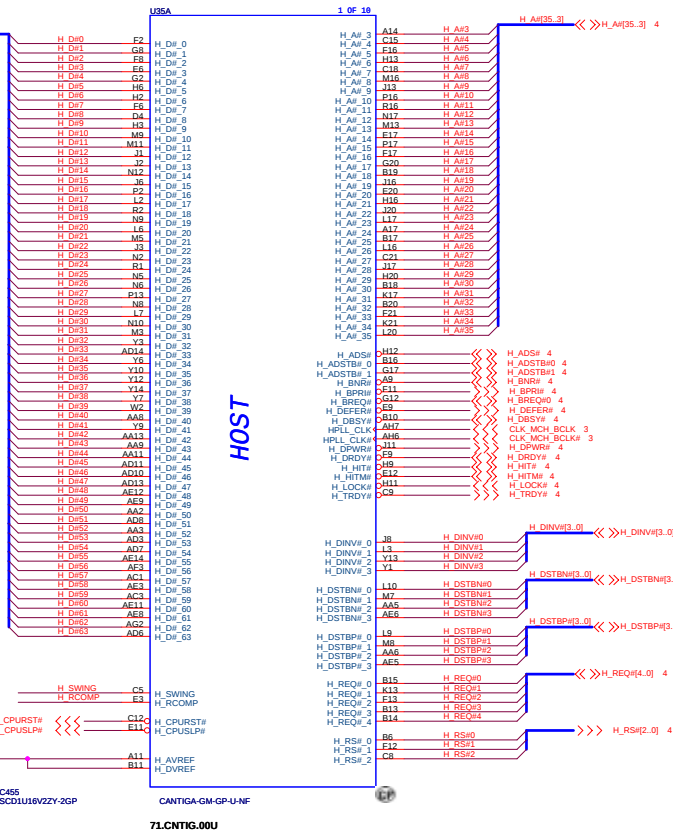
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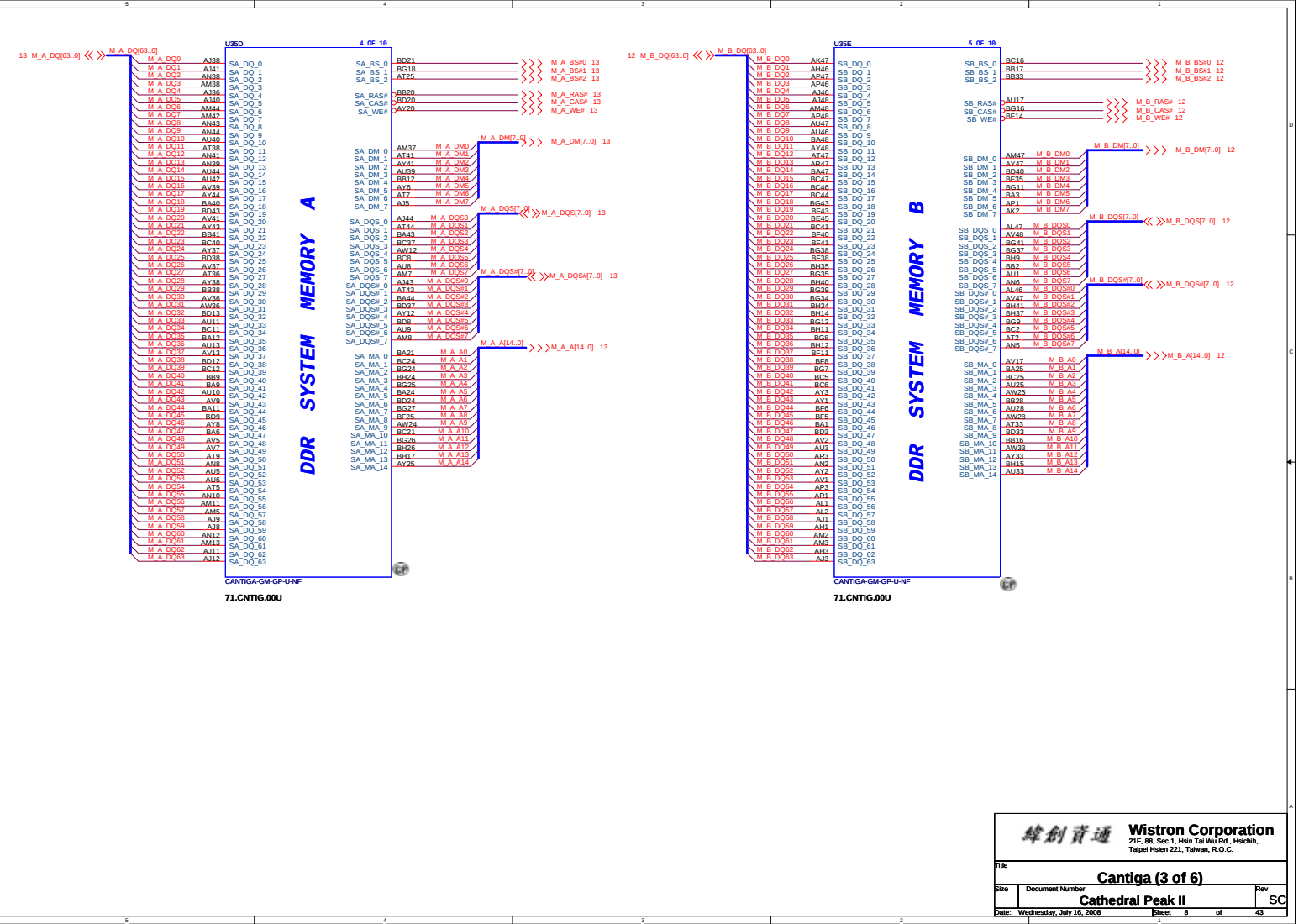
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

File		CPU (1 of 2)	
Size	Document Number	Rev	
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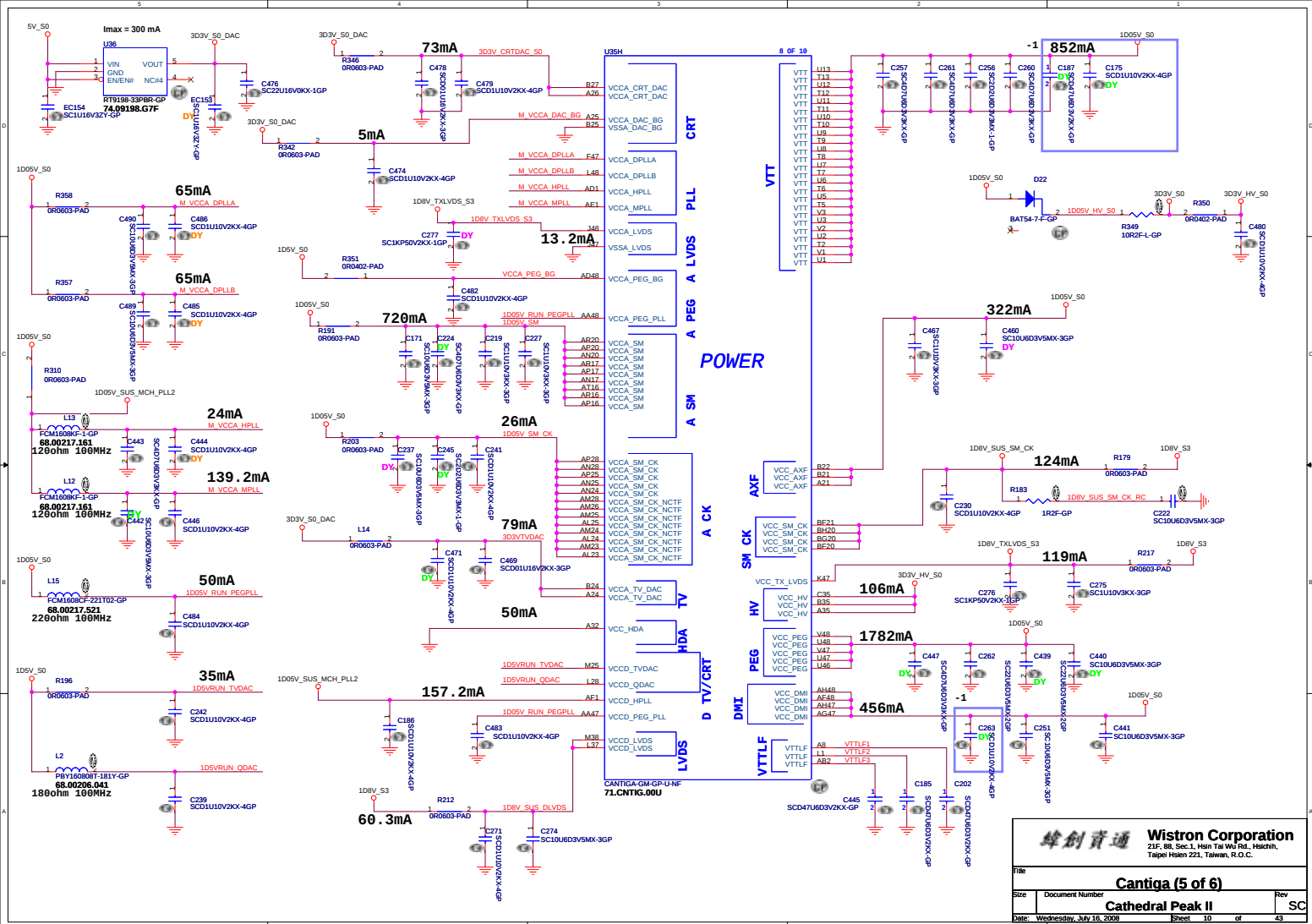


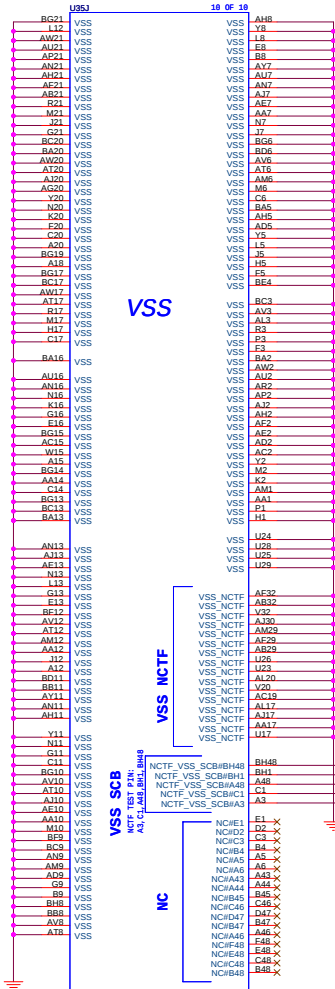
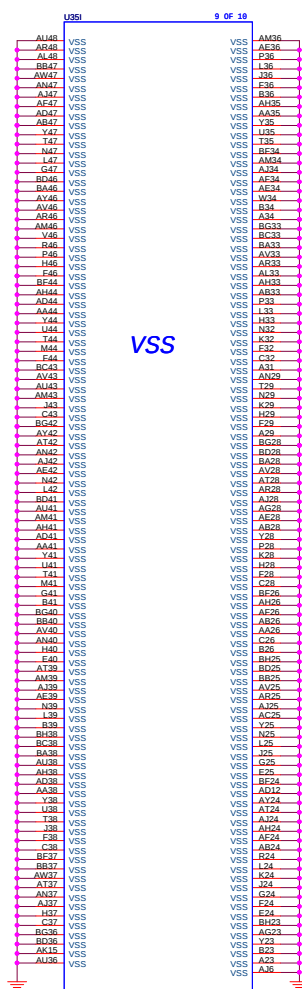
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

[illegible]



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The diagram shows the timing of the VREF_53 signal relative to the clock (CP) for various memory banks. The signal is high for most banks and low for others. The timing parameters are as follows:

Bank	Signal	CP	Parameter	Value
0	High	CP	MEM_A12	2
1	High	CP	MEM_A13	2
2	High	CP	MEM_A14	2
3	High	CP	MEM_A15	2
4	High	CP	MEM_A16	2
5	High	CP	MEM_A17	2
6	High	CP	MEM_A18	2
7	High	CP	MEM_A19	2
8	High	CP	MEM_A20	2
9	High	CP	MEM_A21	2
10	High	CP	MEM_A22	2
11	High	CP	MEM_A23	2
12	High	CP	MEM_A24	2
13	High	CP	MEM_A25	2
14	High	CP	MEM_A26	2
15	High	CP	MEM_A27	2
16	High	CP	MEM_A28	2
17	High	CP	MEM_A29	2
18	High	CP	MEM_A30	2
19	High	CP	MEM_A31	2
20	High	CP	MEM_A32	2
21	High	CP	MEM_A33	2
22	High	CP	MEM_A34	2
23	High	CP	MEM_A35	2
24	High	CP	MEM_A36	2
25	High	CP	MEM_A37	2
26	High	CP	MEM_A38	2
27	High	CP	MEM_A39	2
28	High	CP	MEM_A40	2
29	High	CP	MEM_A41	2
30	High	CP	MEM_A42	2
31	High	CP	MEM_A43	2
32	High	CP	MEM_A44	2
33	High	CP	MEM_A45	2
34	High	CP	MEM_A46	2
35	High	CP	MEM_A47	2
36	High	CP	MEM_A48	2
37	High	CP	MEM_A49	2
38	High	CP	MEM_A50	2
39	High	CP	MEM_A51	2
40	High	CP	MEM_A52	2
41	High	CP	MEM_A53	2
42	High	CP	MEM_A54	2
43	High	CP	MEM_A55	2
44	High	CP	MEM_A56	2
45	High	CP	MEM_A57	2
46	High	CP	MEM_A58	2
47	High	CP	MEM_A59	2
48	High	CP	MEM_A60	2
49	High	CP	MEM_A61	2
50	High	CP	MEM_A62	2
51	High	CP	MEM_A63	2
52	High	CP	MEM_A64	2
53	High	CP	MEM_A65	2
54	High	CP	MEM_A66	2
55	High	CP	MEM_A67	2
56	High	CP	MEM_A68	2
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61	High	CP	MEM_A73	2
62	High	CP	MEM_A74	2
63	High	CP	MEM_A75	2
64	High	CP	MEM_A76	2
65	High	CP	MEM_A77	2
66	High	CP	MEM_A78	2
67	High	CP	MEM_A79	2
68	High	CP	MEM_A80	2
69	High	CP	MEM_A81	2
70	High	CP	MEM_A82	2
71	High	CP	MEM_A83	2
72	High	CP	MEM_A84	2
73	High	CP	MEM_A85	2
74	High	CP	MEM_A86	2
75	High	CP	MEM_A87	2
76	High	CP	MEM_A88	2
77	High	CP	MEM_A89	2
78	High	CP	MEM_A90	2
79	High	CP	MEM_A91	2
80	High	CP	MEM_A92	2
81	High	CP	MEM_A93	2
82	High	CP	MEM_A94	2
83	High	CP	MEM_A95	2
84	High	CP	MEM_A96	2
85	High	CP	MEM_A97	2
86	High			

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

The diagram illustrates the placement of decoupling capacitors (100nF) near the power pins of a 74VHC00 inverter chain. A pull-up resistor (10k) is connected to the input of the first inverter. The power supply is connected to the VCC pin of the first inverter, and the ground is connected to the GND pin. The decoupling capacitors are placed near the power pins of each inverter in the chain.

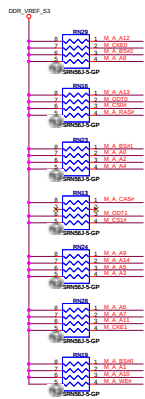
Pinout diagram of the 62.10017.A75 connector, showing 40 pins and their functions. The diagram is divided into two sections: 'REVERSE TYPE' (pins 1-20) and 'REVERSE TYPE' (pins 21-40). Pins 1-20 are labeled with M_B signals (M_B_000 to M_B_019) and M_B signals (M_B_020 to M_B_039). Pins 21-40 are labeled with M_B signals (M_B_040 to M_B_059) and M_B signals (M_B_060 to M_B_079). The diagram also shows the connection of the connector to a 62.10017.A75 connector, which is connected to a 62.10017.A75 connector. The diagram includes a 10k resistor and a 10k resistor connected to the connector pins.

Place these Caps near DM1

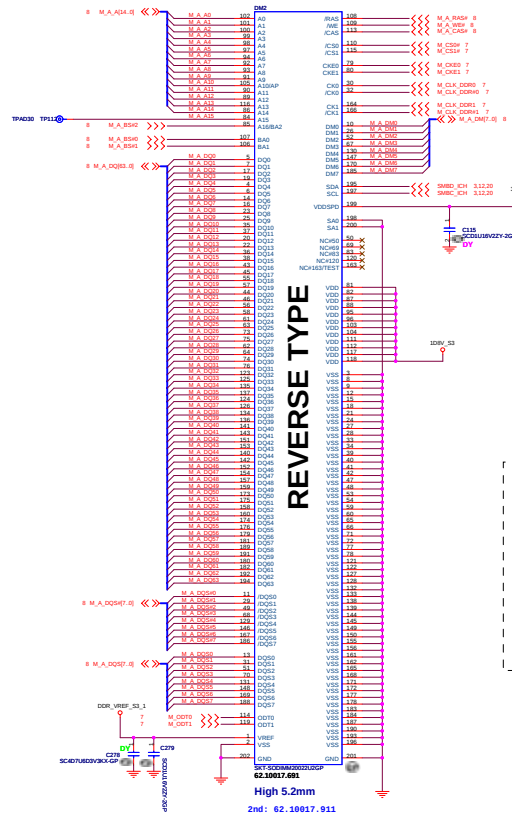
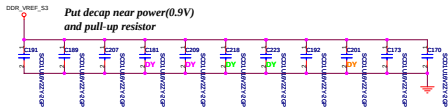
ISSN 0269-9727(200611)14:6

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.			
DDR2 Socket 0 (DM1)			
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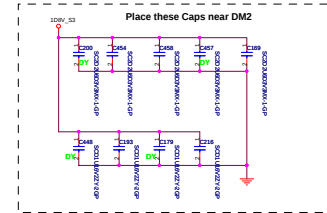
Put decap near power(0.9V) and pull-up resistor



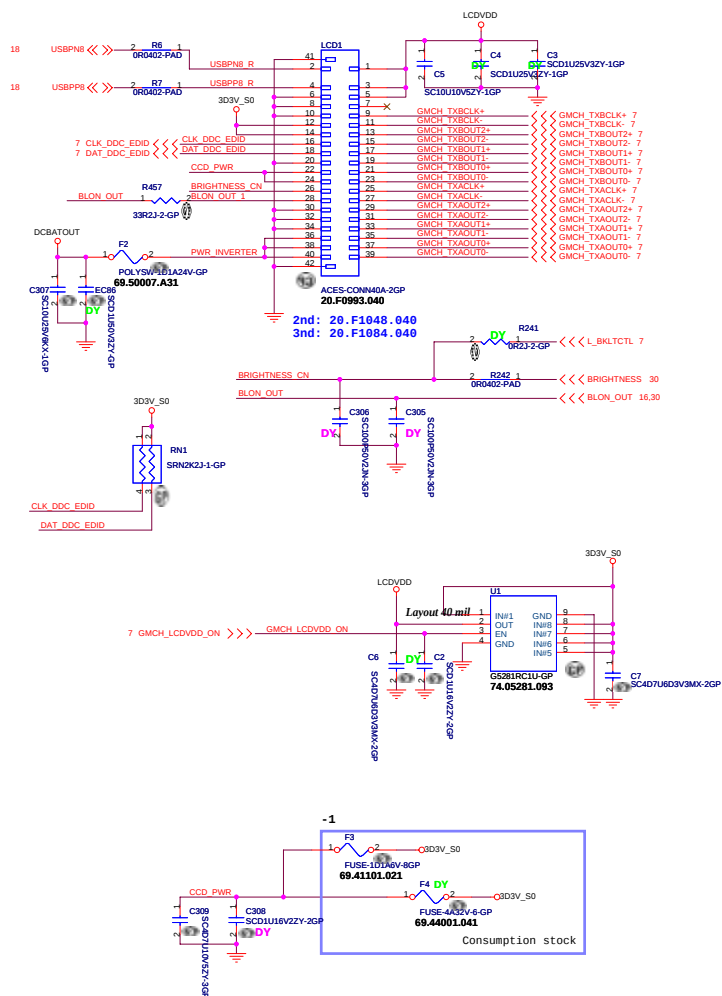
Put decap near power(0.9V)
and pull-up resistor



REVERSE TYPE



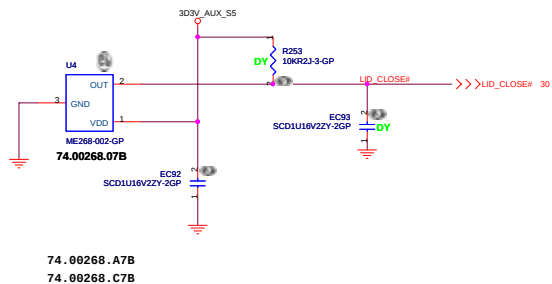
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

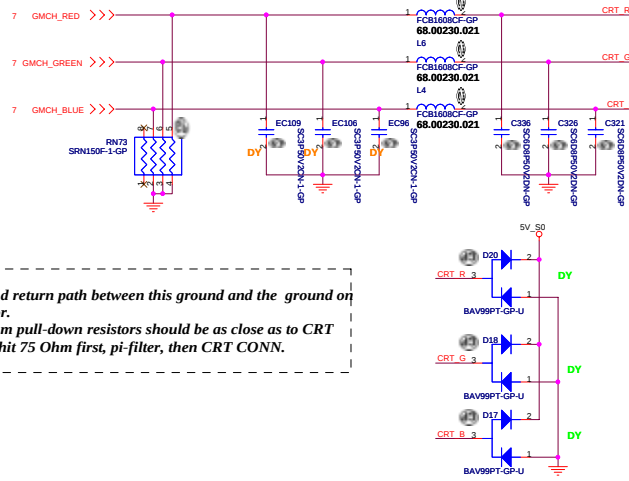
Cover Up Switch



		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD CONN			
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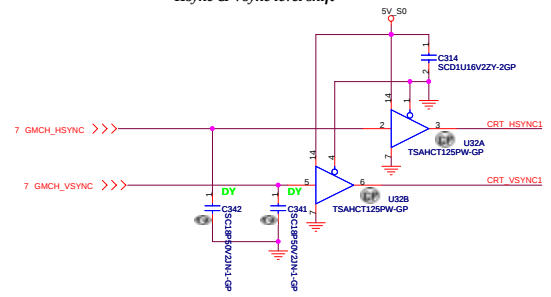
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

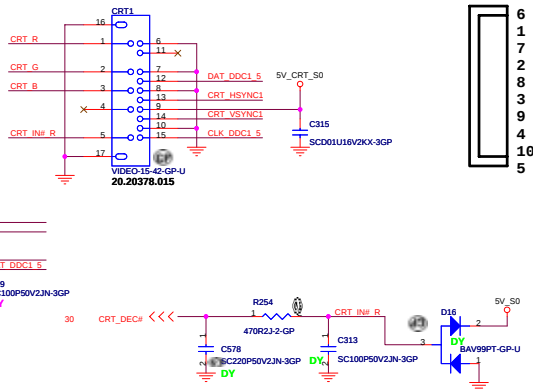


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

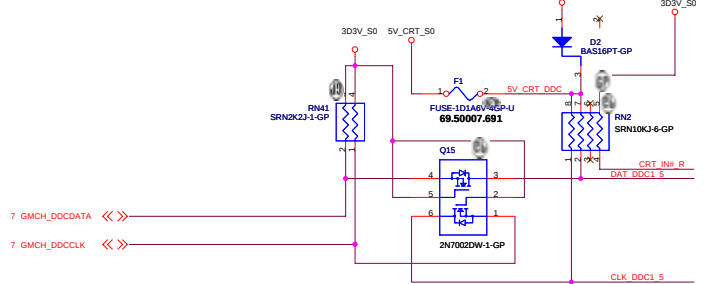
Hsync & Vsync level shift



CRT I/F & CONNECTOR

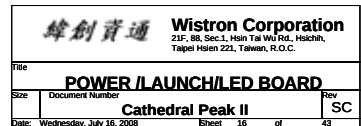


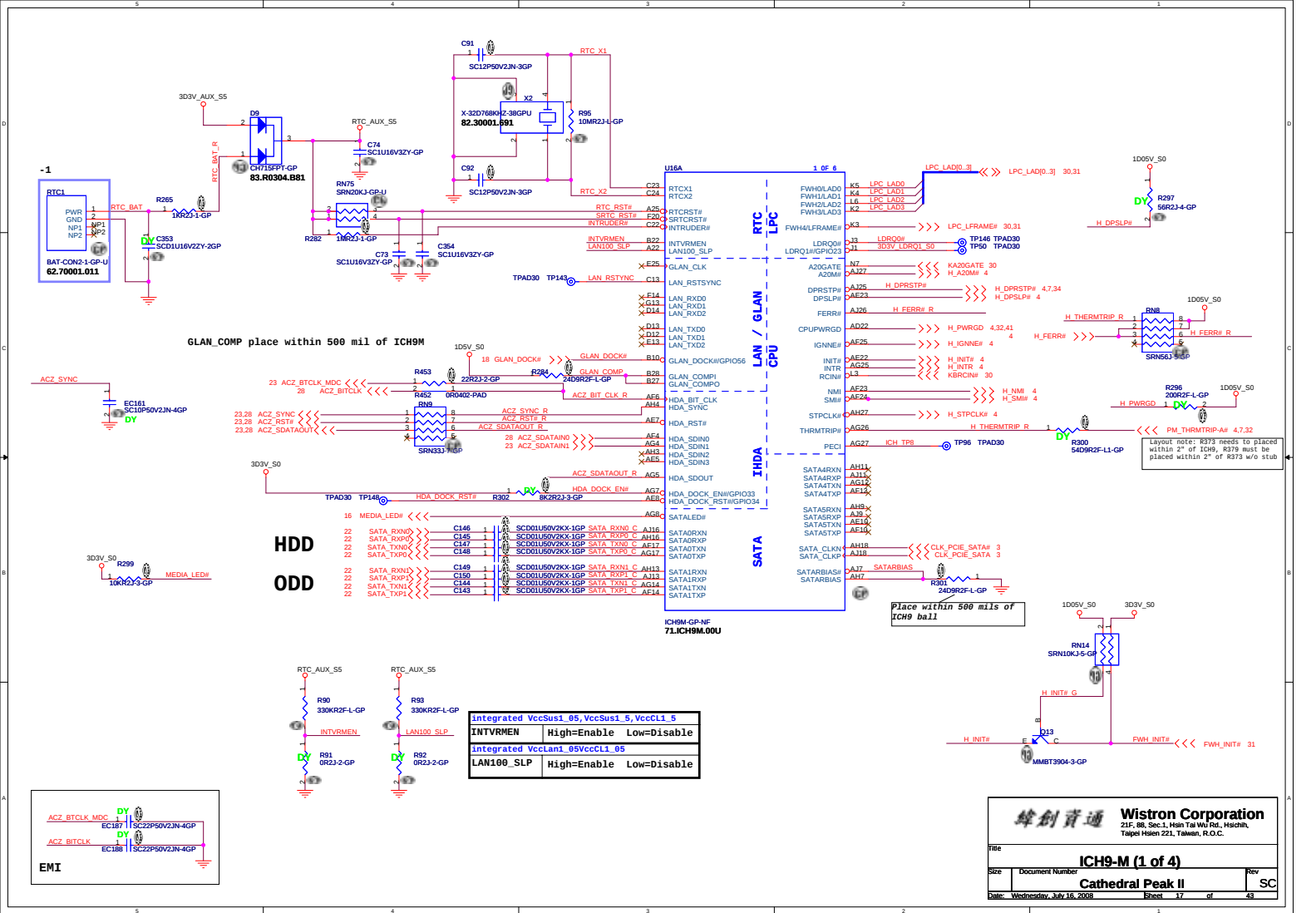
DDC_CLK & DATA level shift

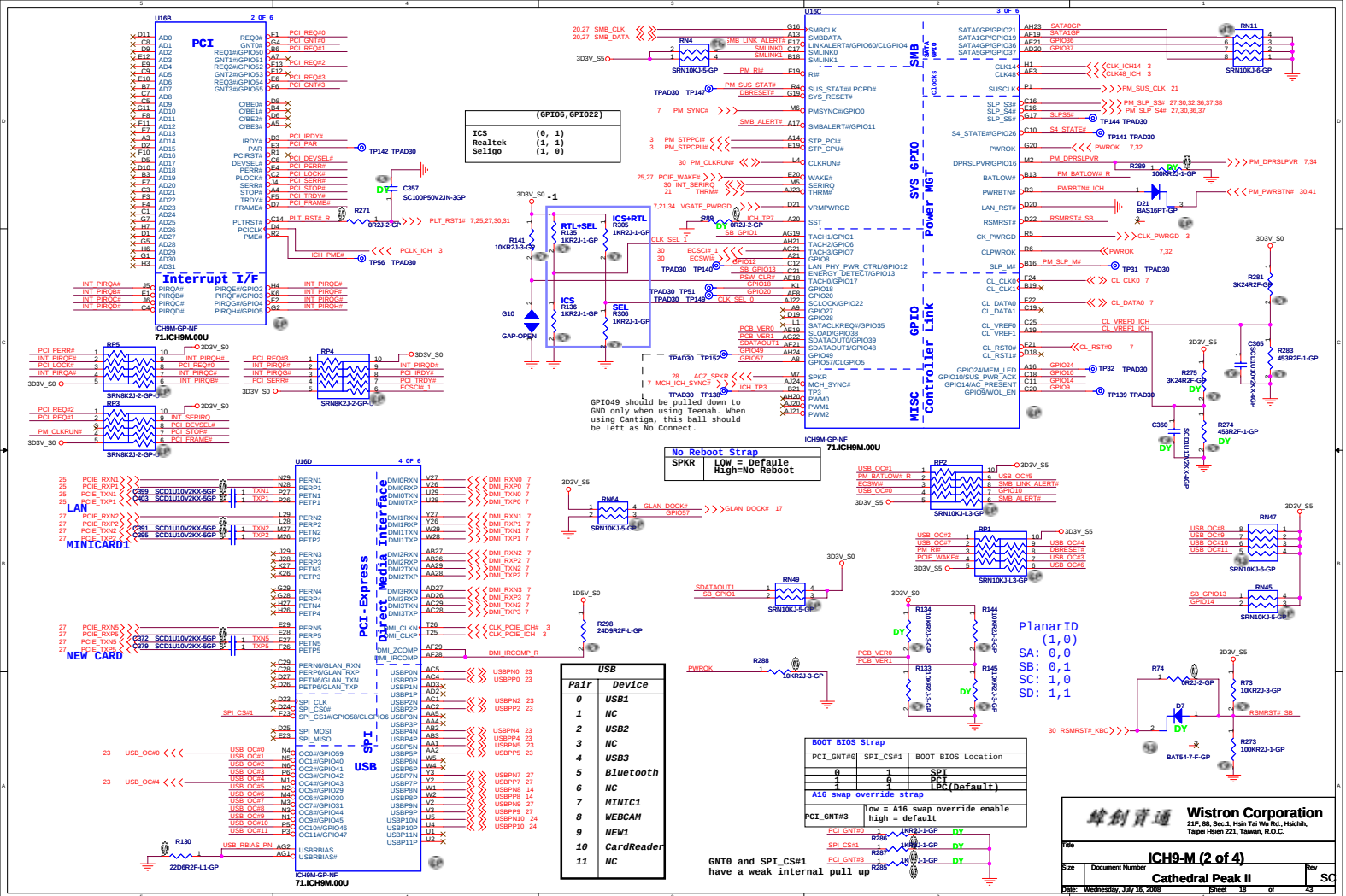


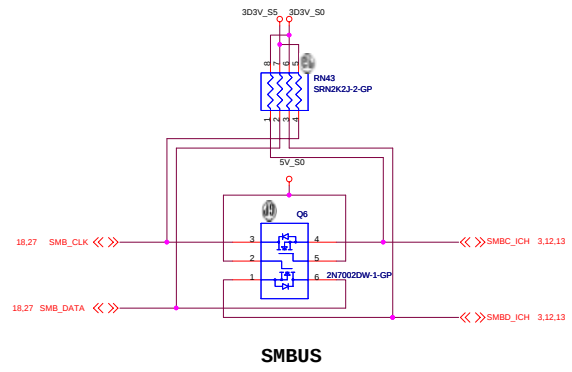
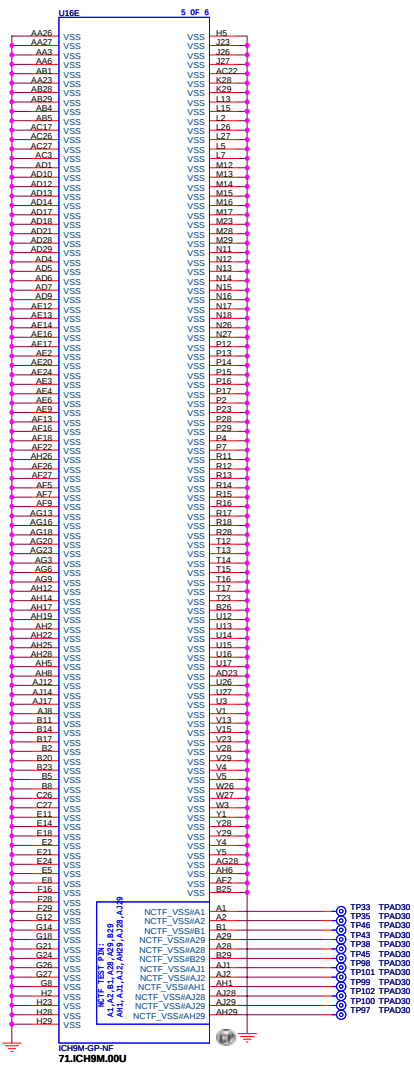
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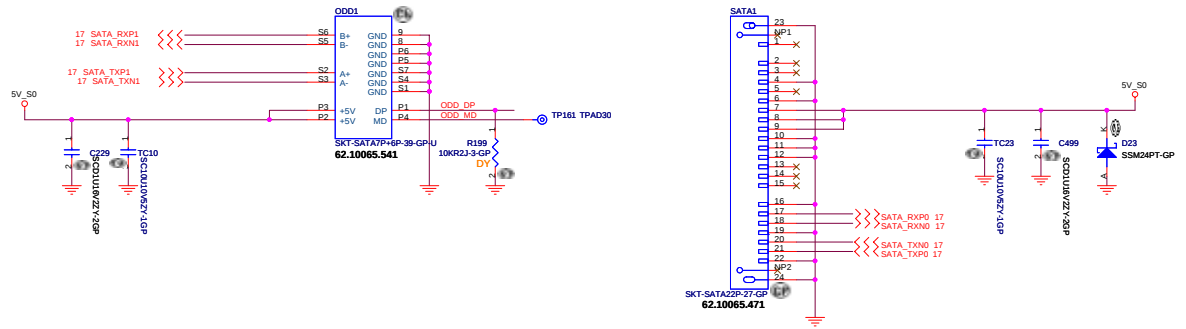


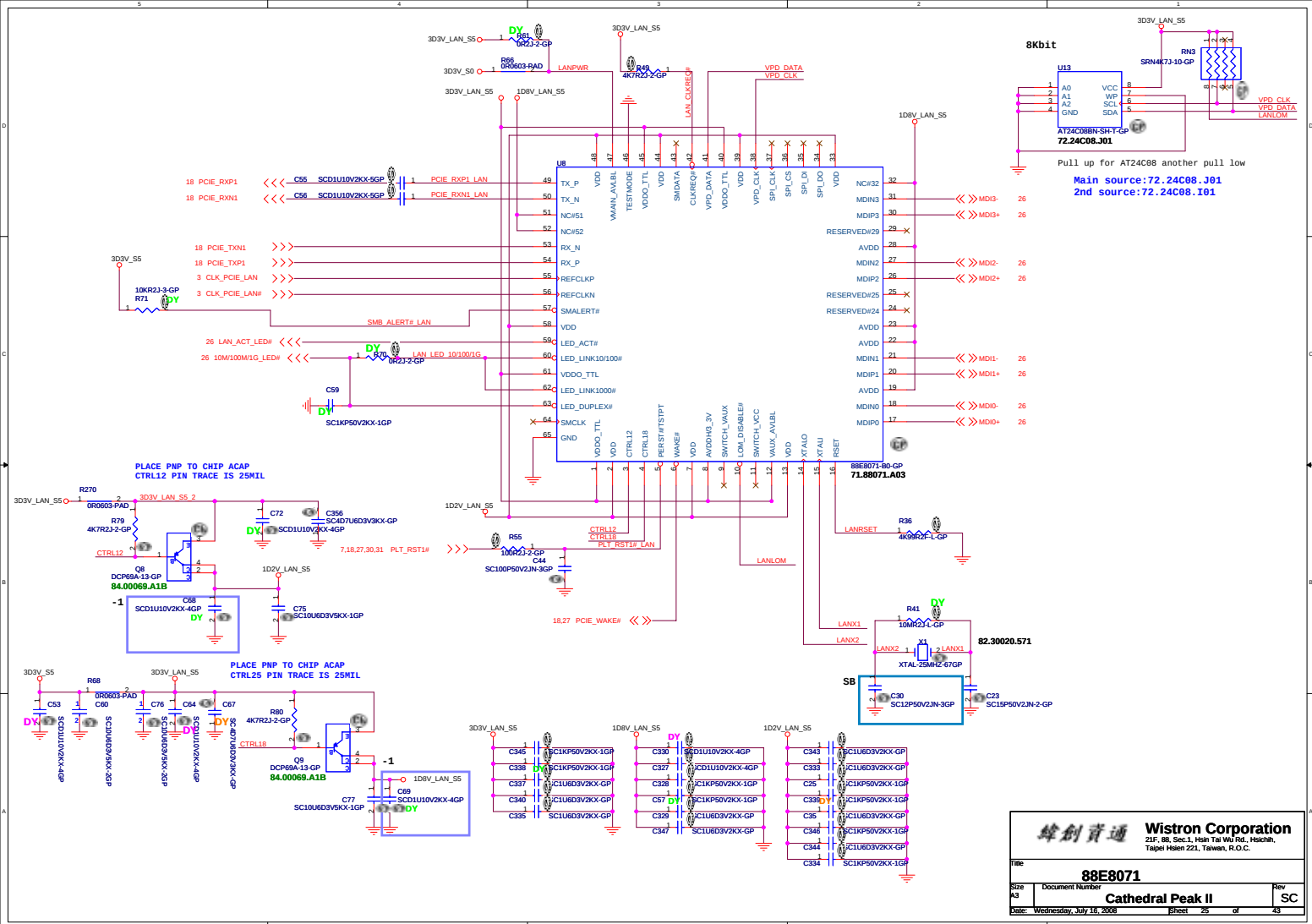




SATA ODD Connector

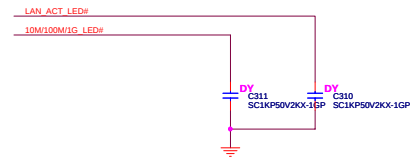
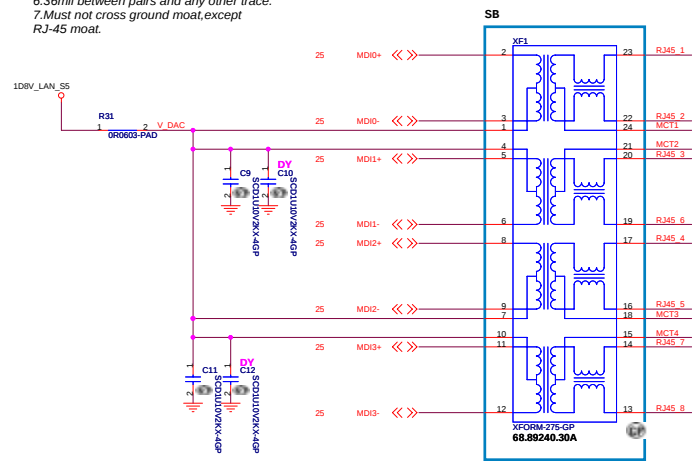
SATA Connector



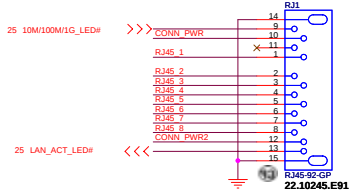


LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+Tx- are pairs. Rx+Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



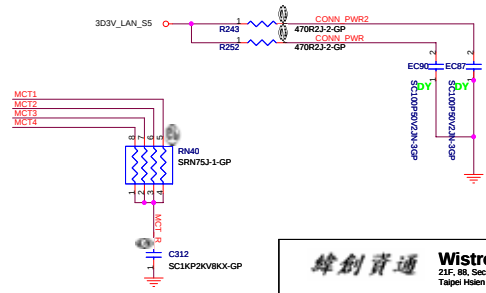
LAN Connector



9:GREEN
13:Orange

LAN Link: Green(9), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(13), when LAN is transferring data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



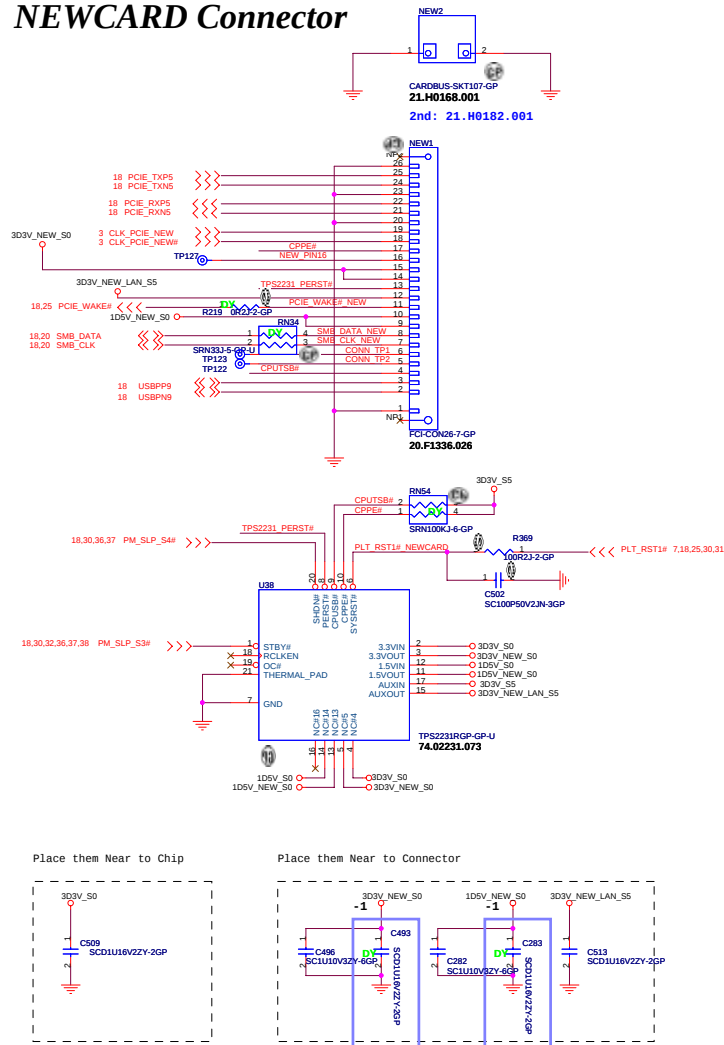
緯創資通

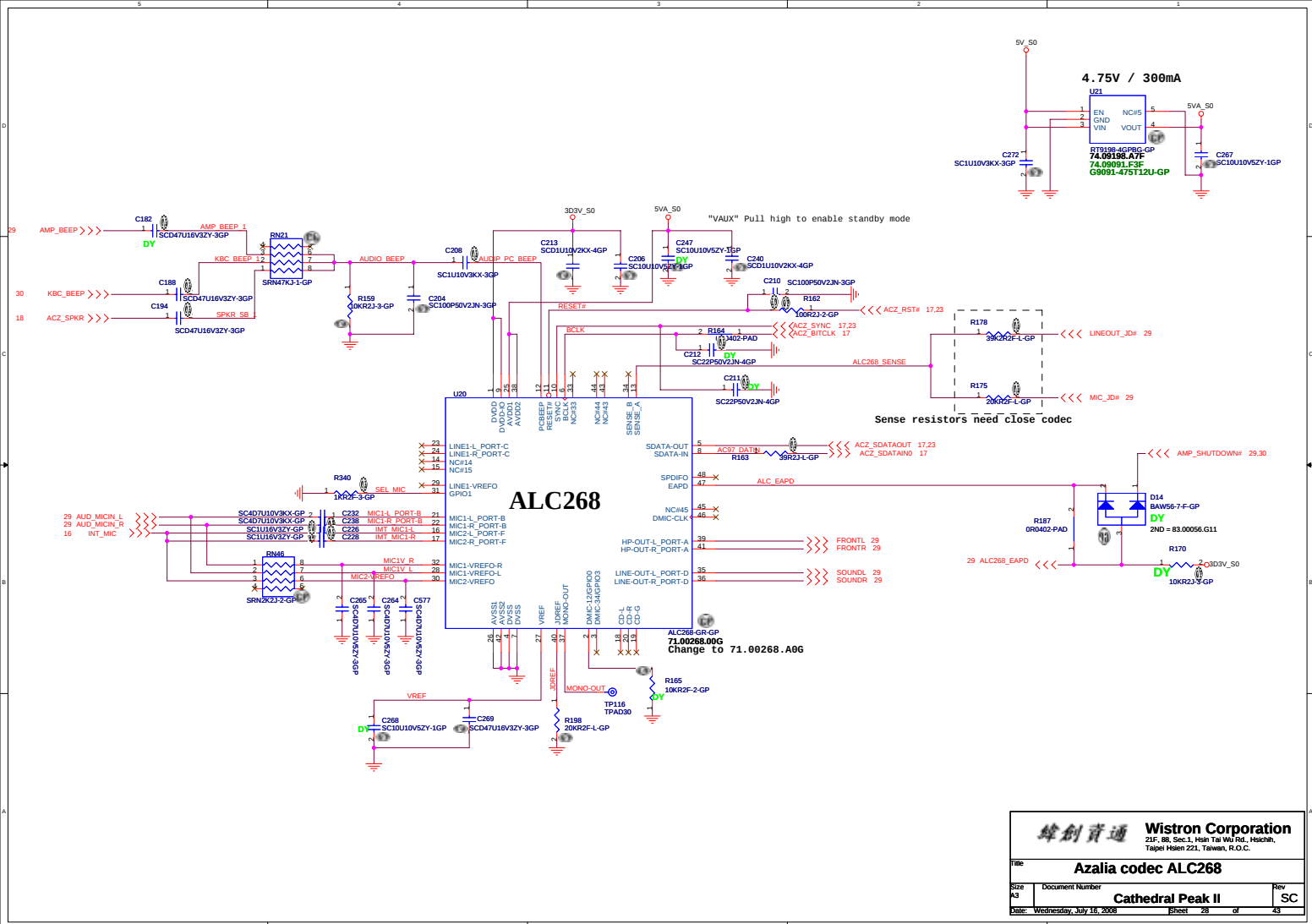
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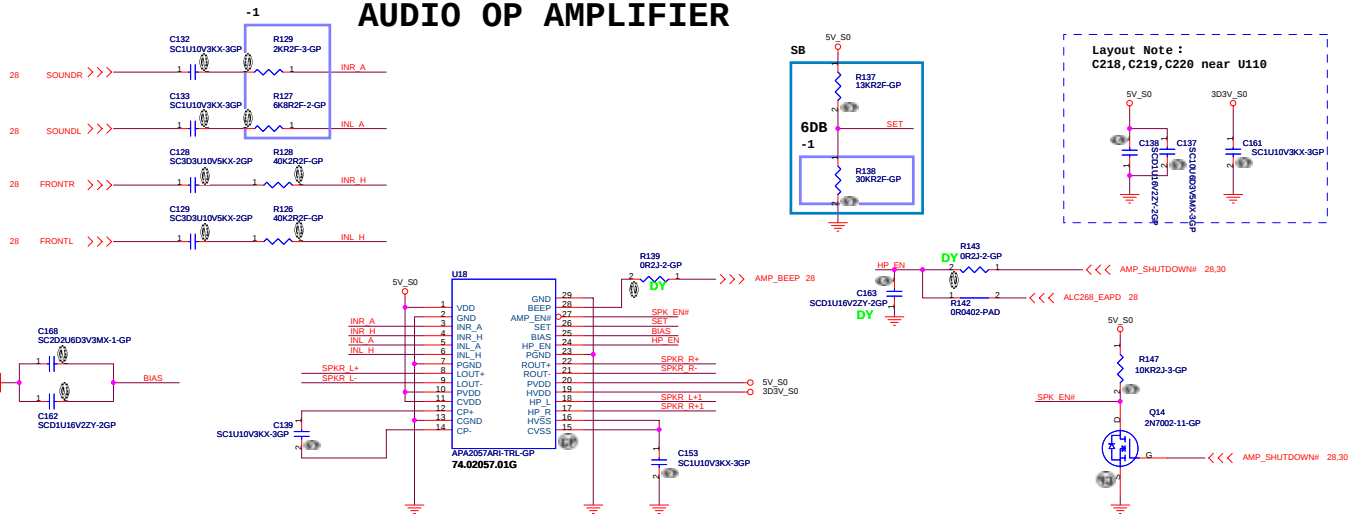
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LAN CONN		
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NEWCARD Connector





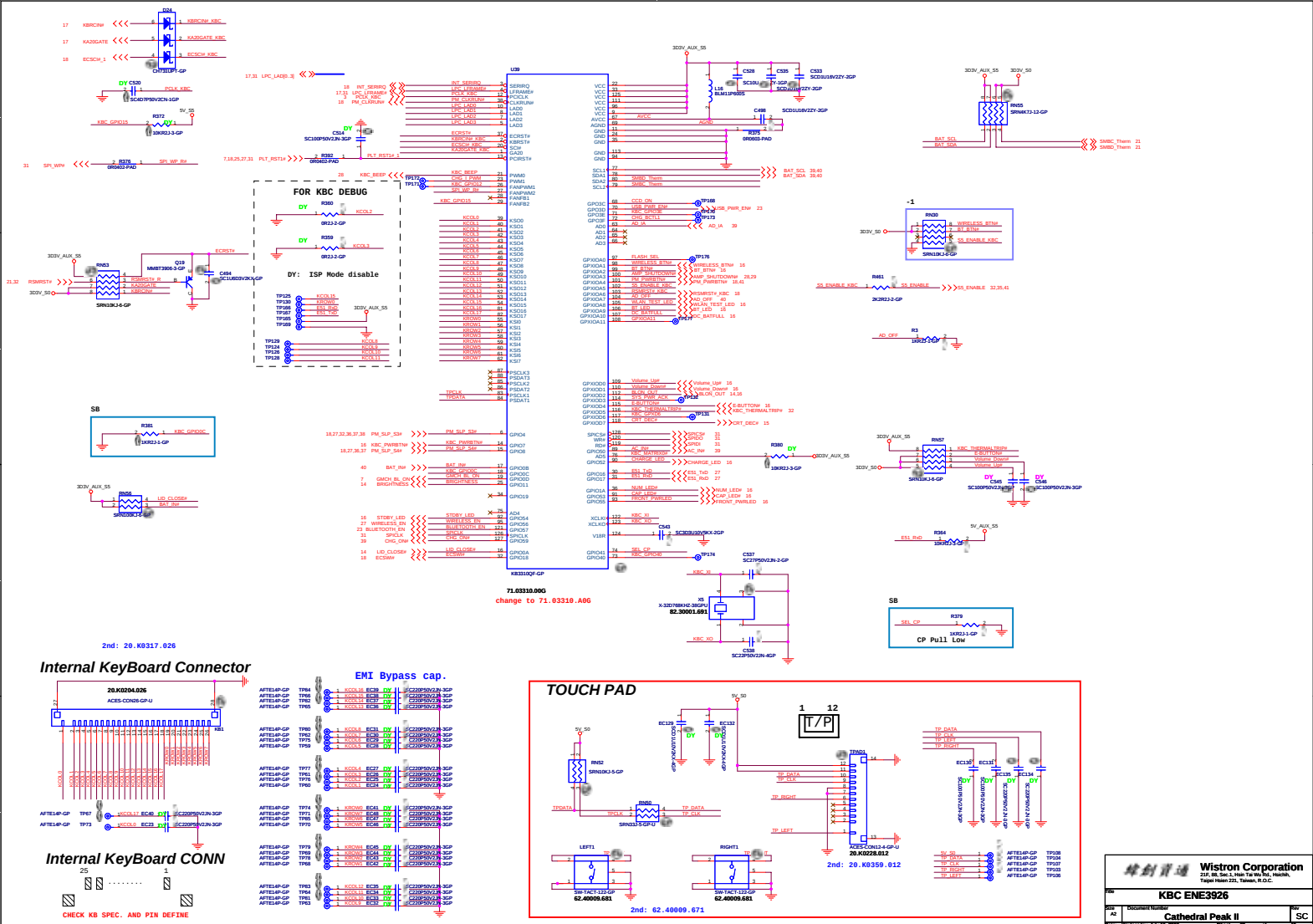
AUDIO OP AMPLIFIER



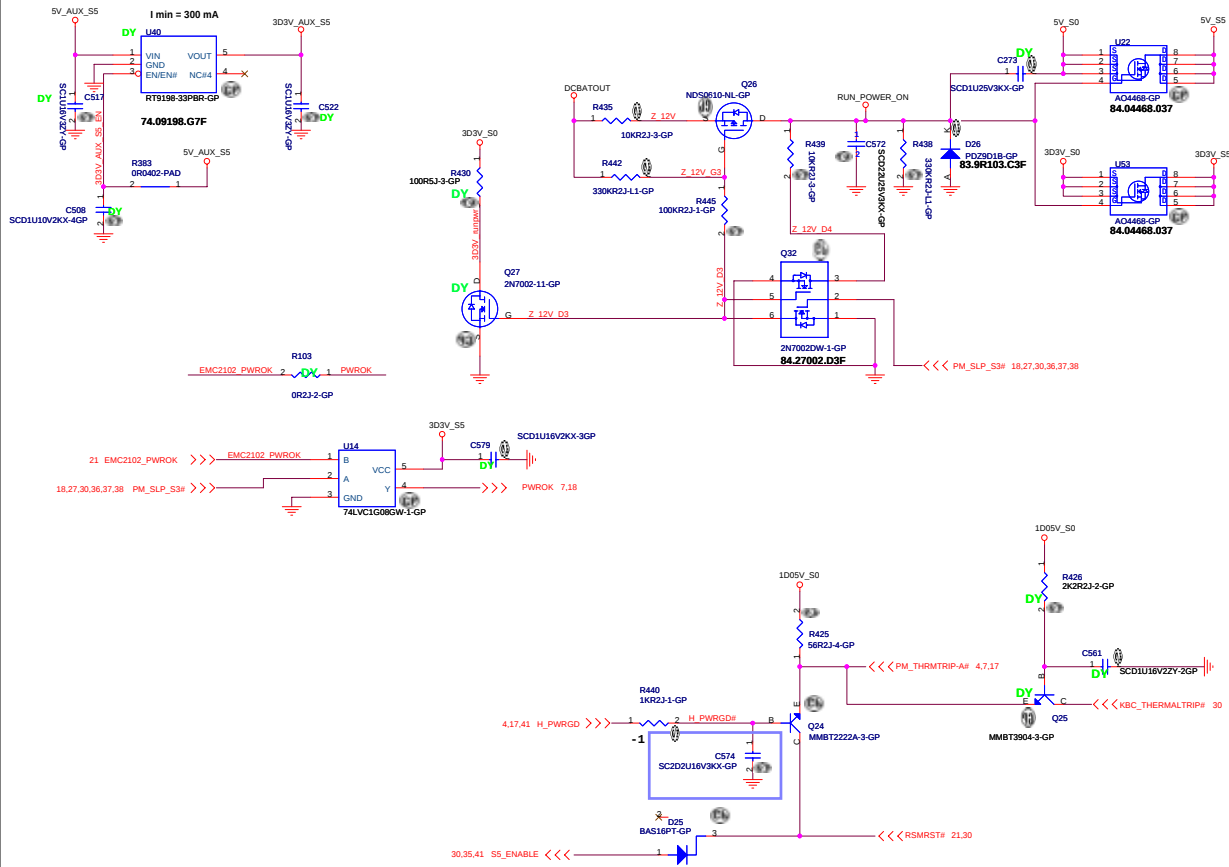
SPKR L-
SPKR L+
SPKR R-
SPKR R+

LINEOUT_3DIF
SPKR R_A1
SPKR L_A1
MIC_INH
AUD_MICIN_R
AUD_MICIN_L

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AUDIO AMP AND JACK	
File	Rev
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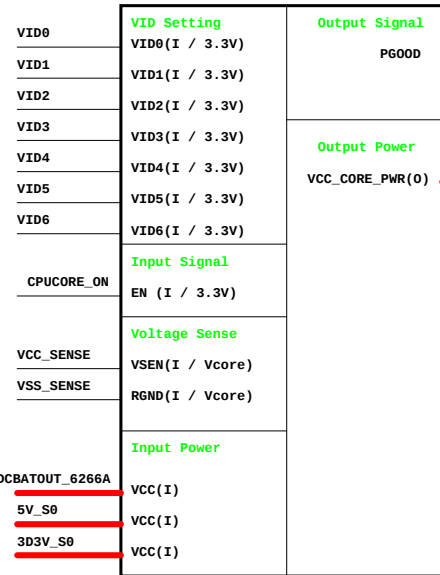




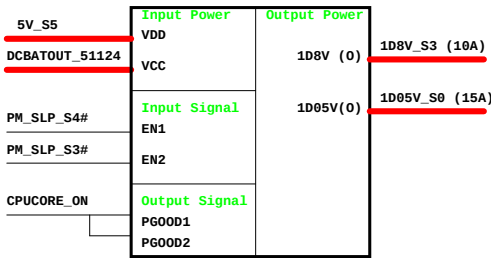


緯創資通 Wistron Corporation 22F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5
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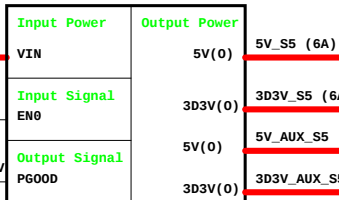
CPU_CORE
ISL6266A



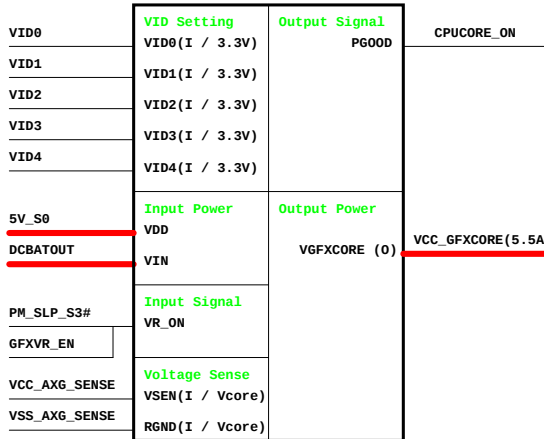
TPS51124
1D8V/1D05V



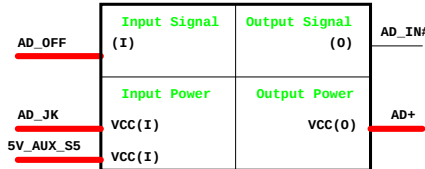
TPS51125
5V/3D3V



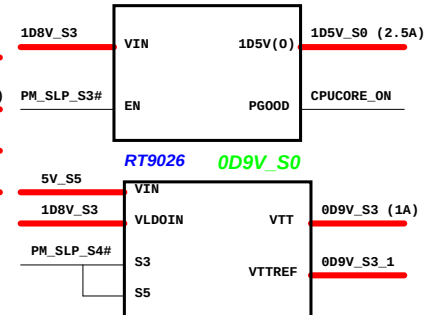
GFX_CORE
ISL6263A



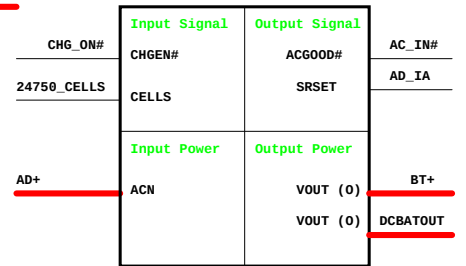
Adapter

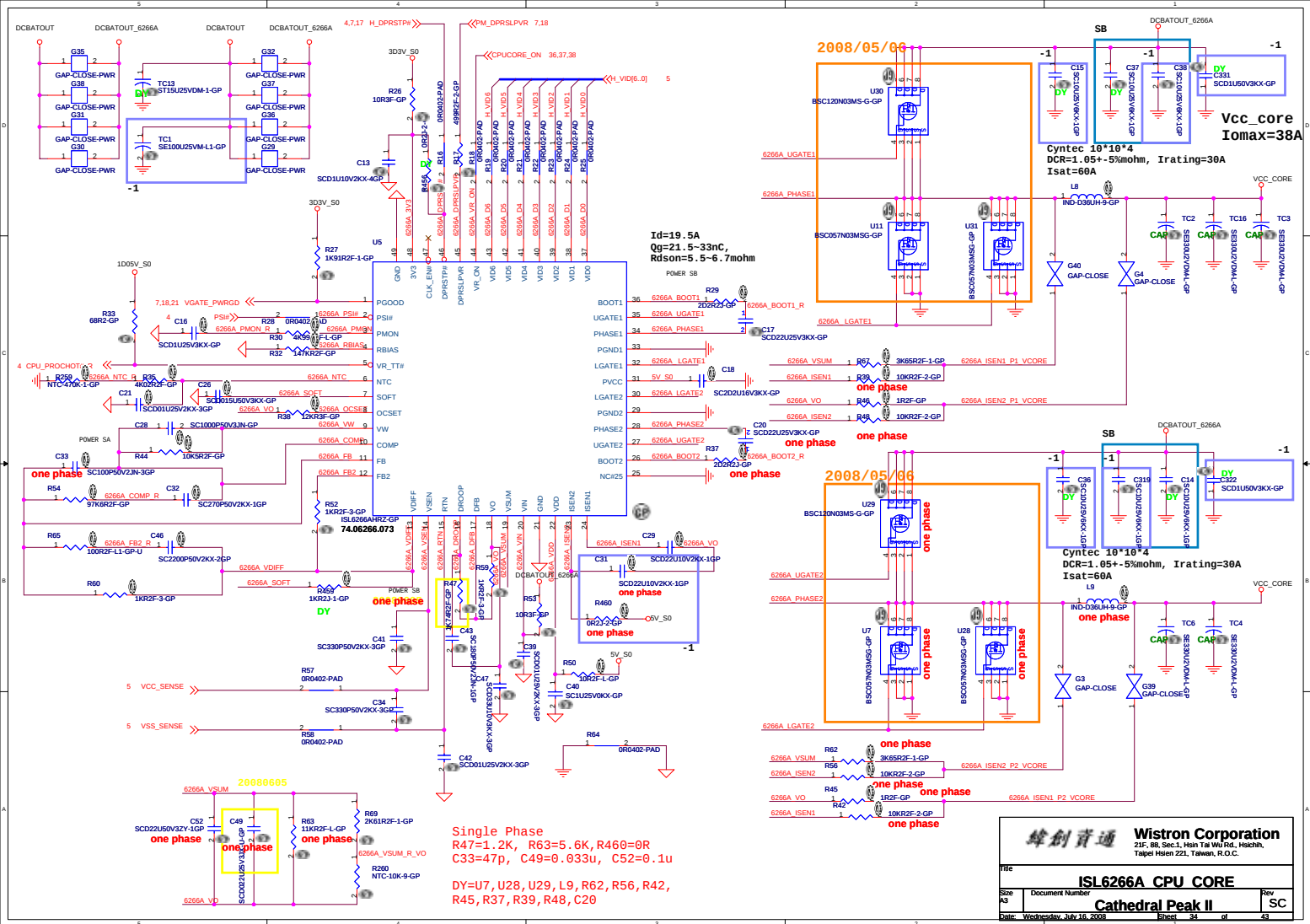


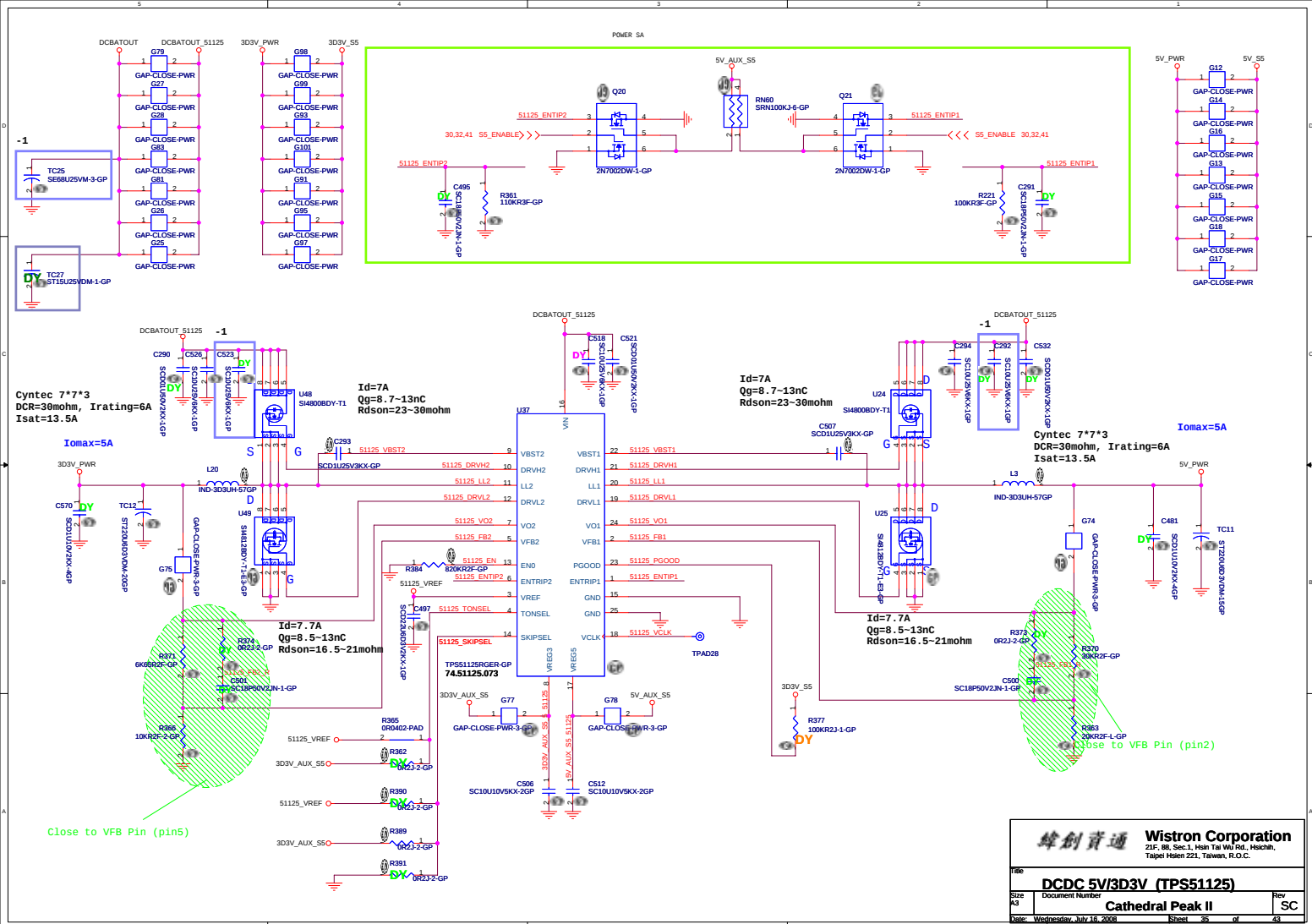
RT9018A
1D5V_S0



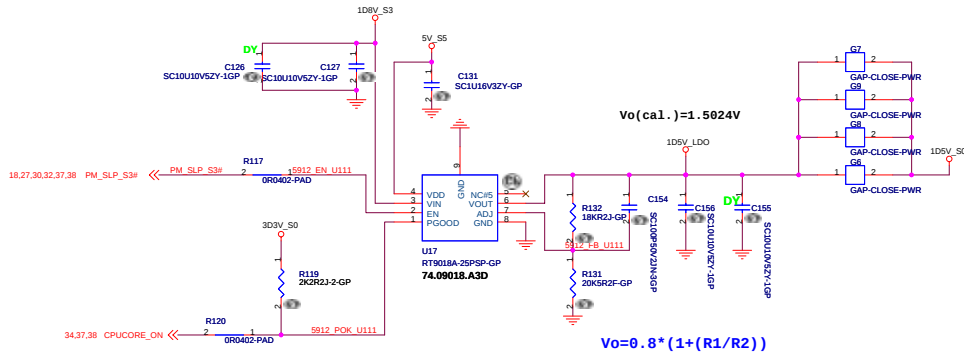
Charger BQ24745



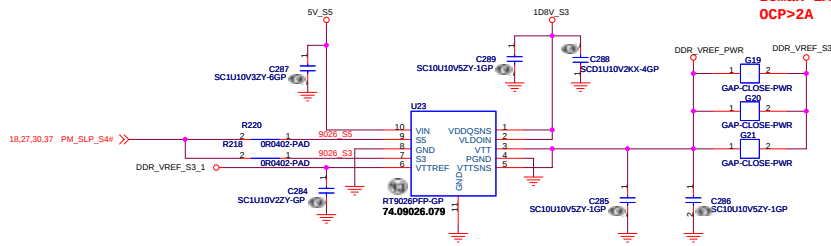




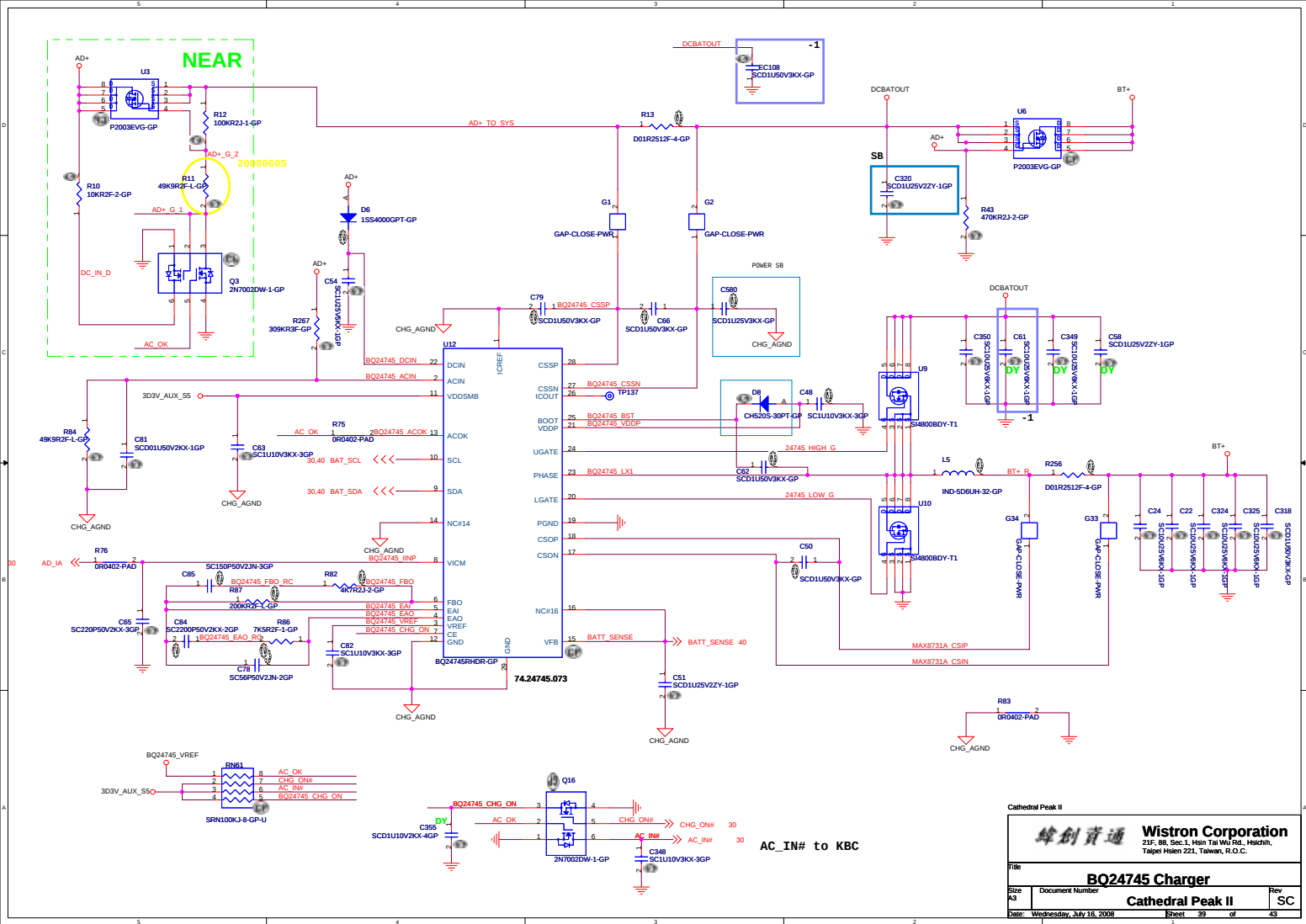
1D5V_S0
Iomax=2.5A



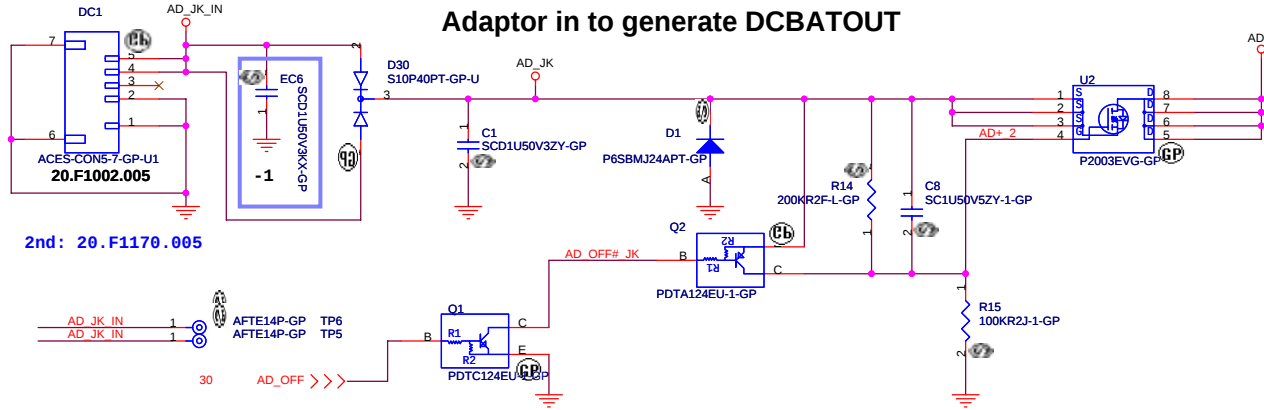
Iomax=1A
OCP>2A



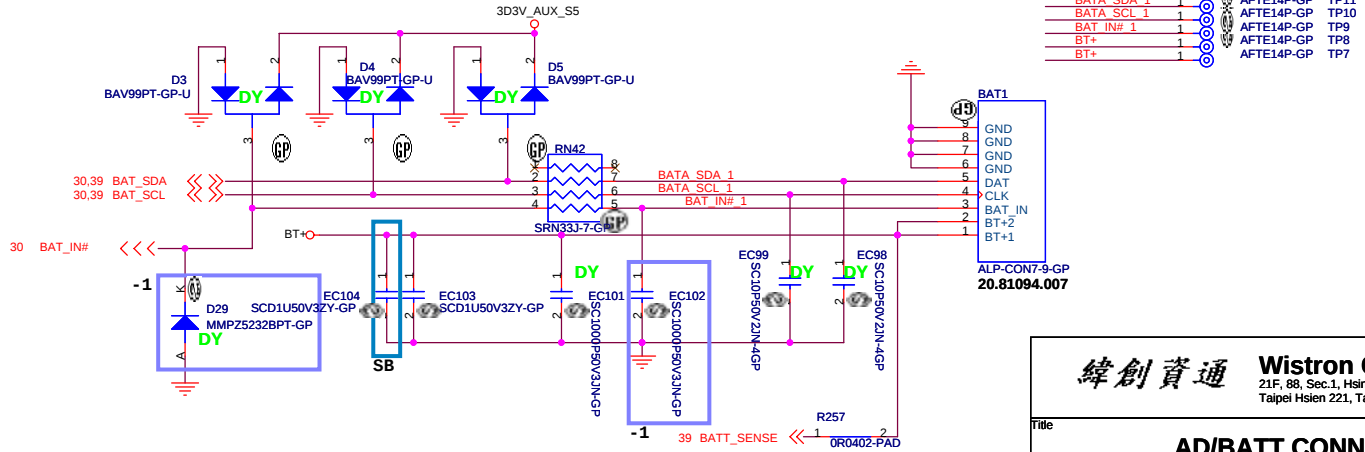
緯創資通		Wistron Corporation 21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D5V & 0D9V			
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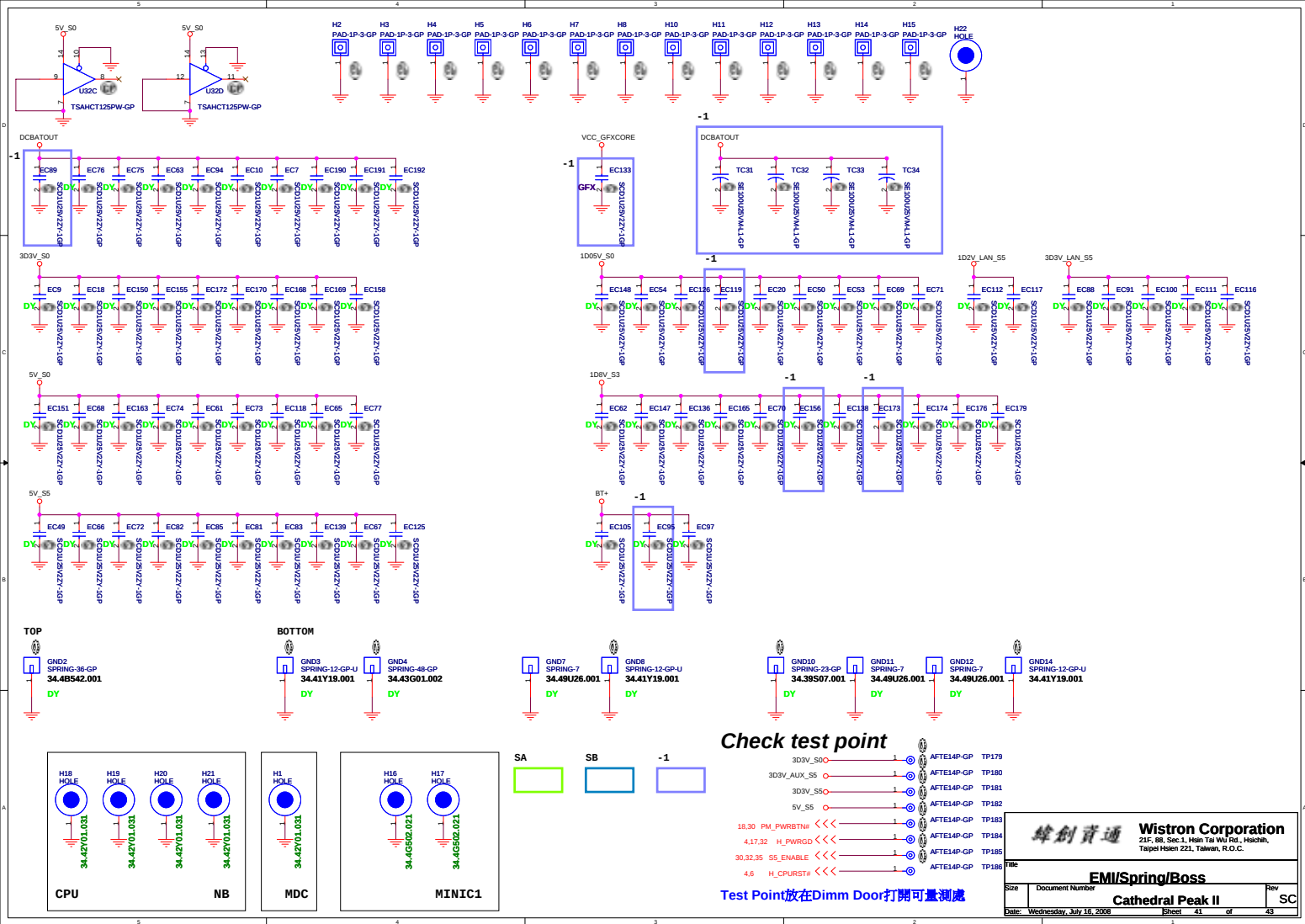
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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AD/BATT CONN	
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SA to SB
1.No Power .
change KBC to B0 (71.03310.A0G)
2.XD Card function fail
Cut CARD1 pin27. connect to R400 pin2
3.leakage
GFX power VDD connect to S0
4.Gain=80db.1.83W R137=16K.R138=30K
5.int.MIC voice to small
add VREF CS77=4.7u
6.Realtek Audio report
change R327=68 ohm.R333=68 ohm.merge to RN68
7.SIV reset
R140=300.R55=100.C44=100p,R398=0,R369=100.C502=100p,R85=300,R162=100.C210=100p,R392=0,
8.SIV Azalia
DY C542
BITCLK rise and fall time fail RN10 change to R453=22ohm(MDC).R452=0ohm(codec)
9.add MINICard power option for customer ask
R454.R455
10.interfere HDD
C390.C401.C419. change 0603 4.7u
11.power team
R38=12K.R47=2.74K .R361=110K.R221=100K.R237=10.7K .R424=20K.R420=17.8K .R227=10.5K
R48=10K.R29=2.2 .R37=2.2 .R401=3.3 .C49=0.1u.add R456.add C500.D8=83.R0203.00F .
TC11 change to 77.C2271.00L
TC9 change to 77.E9071.001 (power ripple)
add R458=1K.R459=1K.R460
12.Oscillation
C30=15p.C23=15p.C537=27p.C538=22p
13.audio S3.S4 resume bobo sound
R143 DY. R187 0ohm pad
14.AC mode have hight frequency noise
R390 DY.R389 0ohm pad
15.ESD issue
BAT_IN# series 33 ohm
RN42 change to 8p4r
add R457.D27.D28.D29.U55.U56.C578.R457.
16.noise
DY C523.TC25 change to 77.C1561.01L
20.LED brightness
R2.R1.R4.R5.R451.R450.R449.R448=56
R2.R1.R4.R5.R451.R450.R449.R448=56
EMI
1.EC23 ---EC48.EC134.EC135.EC167.EC121.EC122.EC123.
2.EC89.EC12.EC8.EC119.EC156.EC173.
3.EC174---EC179.
4.GND13.GND14.
Merge
1.R313.R314.R315.R319.R320.R149. change to RN59
2.RN6.RN46. change to RN6
3.R341.R343.R344 change to RN46
4.R305 change to 100K merge R302 to RN56
5.RN53.RN56. change to RN53
6.Q20.Q21 change to Q21. Q21.Q23 change to Q21.
7.R367.R368 change to RN60
8.Q16.Q17 change to Q16
9.R262.R264.R268.R277 change to RN61
10.R205.R204.R206 change to RN62
11.RN33.R215 change to RN33
12.R209.R210.R340 change to RN63
13.R200=10K.merge R269 to RN64
14.R109.R112.R111.R290 change to RN65
15.R325.R323 change to RN66
16.R304.R307 change to RN67
17.U14 change to 73.01G08.L04 .add C579
18.R51.R399 vchange to RN69.
0 Ohm change to PAD
R427.R403.R415.R413.R411.R408.R404.R146.R197.R157.R153.R353.R352.R358.R357.R310.R196.R346.R342.R351.
R191.R203.L14.R212.R350.R179.R217.R6.R7.R242.R294.R278.R279.R292.R293.R232.R233.R410.R393.
R416.R250.R251.R248.R249.R246.R247.R244.R245.R129.R127.R376.ER2.R383.R28.R16.R19.R20.R21.
R22.R23.R24.R29.R57.R58.R365.R164.

05/05

Page16: merge LAUNCHCN1 LEDCN1 to LAUNCHCN1 15pins

Page15: change CRT1 from 20.20717.015 to 20.20378.015

Page26: change RJ1 from 22.10277.011 to 22.10245.E91

Page23: change BLUE1 from 20.D0197.004 to 20.F0984.004

Page24: change CARD1 from 20.I0081.001 to 20.I0067.001

Page21: change FAN1 from 20.F0714.003 to 20.F1000.003

Page27: change MINIC1 from 20.F1049.052 to 62.10043.331

Page30: change TPAD1 from 20.K0286.012 to 20.K0174.012

Page34: change U29 U30 from 84.07686.037 to 84.12003.A37 and change U7 U11 U28 U31 from 84.04634.037 to 84.57N03.A37

Page16: delete LED1 LED2 R1 R2 R4 R5

05/07

Page17: change RTC1 from 62.70001.011 to 20.F0700.003

Page41: delete EC51

Page10: delete C159

Page25: change U13 from 72.24256.R01 to 72.24C08.J01

05/08

Page30: change KB1 from 20.K0127.026 to 20.K0204.026

Page26: delete RN36 RN37 RN38 RN39

Page23: change TC28 from 80.15715.34L to 77.C1071.081

Page26: change TC15 from 80.15715.34L to 80.15715.12L

Page23: delete R244 R245 R246 R247 R248 R249 R250 R251

Page24: change CARD1 from 20.0067.001 to 20.I0079.001

05/09

Page41: delete GND13

05/12

Page24: add EC127 EC128 EC185 EC186

Page35: change TC27 from 77.C1561.01L to 77.C1561.03L

Page40: change BAT1 from 20.80697.007 to 20.80906.007

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05/13
Page16: change pin1 pin2 of LED6 from 3D3V_S5 to 3D3V_AUX_S5

05/14
Page17: add EC187 EC188

Page16: add EC189 TP189~TP195

Page30: change TPA1 from 20.K0174.012 to 20.K0228.012

Page41: add EC190~EC195

05/15
Page17: change U15 pin13 pin14 from pull high 3D3V_S0 to VGATE_PWRGD

Page17: change Q11 6 from 3D3V_S0 to VGATE_PWRGD

Page40: change D1 from 83.P4SSM.BAM to 83.P6SBM.AAG

S8
05/15
Page30: change KBC_GPI00C from pull-high 3D3V_AUX_S5 with 10K to pull-low GND with 1K

06/06
Page3: change C176 C177 from 78.27034.1FL (27p) to 78.33034.1FL (33p)

Page22: delete D15

Page29: change R127 R129 from 0ohm pad to 12K 1K5 and change R137 R138 from 16K 30K to 13K 20K

Page34: change TC1 from 77.C1561.01L (15u) to 79.10712.L02 (100u) and C14 C37 C38 C319 dummy

Page35: change TC25 from 77.C1561.01L (15u) to 79.68612.30L (68u) and change C292 to dummy

Page37: add TC30 79.68612.30L (68u) and change C553 C563 to dummy

Page38: change C536 to dummy and change TC24 from 77.C1561.01L (15u) to 79.68612.30L (68u)

Page39: change C61 to dummy

Page41: add TC31 TC32 TC33 TC34 and delete GND9

06/09
Page16: add LED3 R458 R465

06/11
Page30: change R379 from 10K to 1K

06/13
Page3: add EC59 DY

06/13
Page37: change R446 R447 from 0ohm pad to 0ohm resistor

Page26: change XF1 from 68.69241.301 to 68.89240.30A

06/17
Page39: C320 mount

Page40: EC104 mount

Page41: EC95 mount

Page39: change R11 from 10K to 49K9

Page34: change C49 from 47nF to 22nF and change R47 from 2.74K to 1.74K

Page37: add C581 C582

Page41: delete GND6

06/20
Page25: change C30 from 15p to 12p

SC
06/30
Page37: change R446 R447 from 0ohm resistor to 0ohm pad

07/07
Page3: change C462 to DY

Page16: change EC22 to DY

Page21: change C109 to DY

Page40: change D29 to DY

Page10: change C187 C175 C263 to DY

Page12: change C166 to DY

Page19: change C396 C407 to DY

Page25: change C68 C69 to DY

Page40: change EC102 to DY

Page41: change EC89 EC119 EC156 EC173 to DY

Page24: change C529 to DY

Page27: change C283 C493 to DY

Page30: delete R397, S5_ENABLE_KBC connect to RN30 PIN5, RN30 PIN4 connect to GND

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Page14: add F3, DY F4

Page34: DY C15 C36, add C319 C38

Page39: change C61 to DY

Page35: change C292 C523 to DY

Page37: change C553 C563 to DY

Page34: change TC1 to mount

Page38: change TC24 to GFX

Page35: change TC25 to mount

Page37: change TC30 to mount

Page41: change TC31 TC32 TC33 TC34 to mount

07/09

Page34: change C322 C331 from DY to mount

Page39: change EC108 from DY to mount

Page40: change EC6 from DY to mount

07/10

Page18: DY R136 R305 for ICS, DY R135 R305 for RTL

Page16: change LAUNCHCN1 to 2nd source

Page3: change EC59 from 5p DY to 22p mount

07/10

Page17: change RTC1 from 20.F0700.003 to 62.70001.011

Page32: change C574 from 1u to 2.2u

07/16

Page41: change EC95 to DY

Page34: change C331 C322 to DY

Page40: change EC102 to mount

Page41: change EC89 EC119 EC173 to mount

Page41: change EC133 to mount on GM45

Page29: change R127 from 12K to 6.8K, change R129 from 1.5K to 2K, change R138 from 20K to 30K

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